

**Design of Fir Filter Using Area and Power Efficient Truncated Multiplier**

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**Abstract**

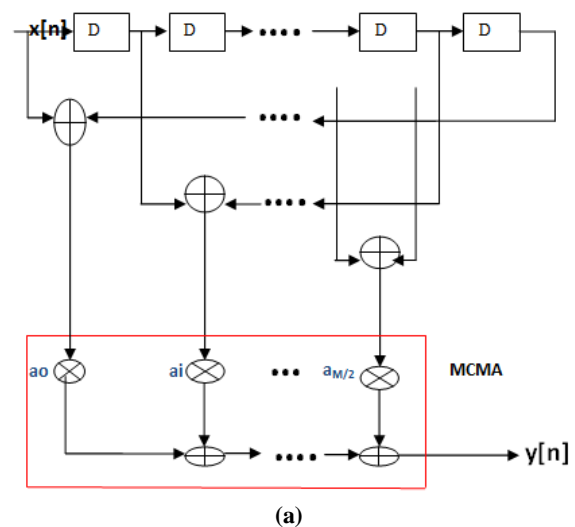
This paper describes the design of Finite Impulse Response (FIR) using the rounded truncated multiplier which offers diminution in area, delay, and power. This anticipated method finally reduces the number of full adders and half adders during the tree reduction in the multiplier block. LSB and MSB is the output form of this multiplier. Deletion, reduction, truncation, rounding and final addition are the operations performed to compress the LSB part. When this scheme is followed the truncation error does not exceeds 1 ulp (unit of least position). So it does not necessitate any error compensation circuits, and the final output will be precised. The proposed filter using truncated multiplier will be designed using VHDL and simulated using ISE Simulator (ISIM).It achieves best area and power result when compared with previous FIR design approaches.

**General Terms:** Digital signal processing, bit width optimization, VLSI design.

**Keywords:** Finite impulse response (FIR) filter, truncated multiplier, partial product(PP), carry propagate adder(CPA), flip-flop, ulp

**Introduction**

Finite impulse response (FIR) digital filter is a major component in digital signal processing(DSP) and applications of communication systems. As it offers limited area and power it is widely used in many portable applications. The two basic FIR structures for a linear phase FIR filter are direct form and transposed form as shown in Figure 1. As shown in Fig 1(a), which is the direct form, the multiple constant multiplication (MCM), multiple constant multiplication and accumulation (MCMA) where the concurrent multiplications [1] is performed which involves the individual delayed signals and corresponding filter coefficients which is followed by accumulation of all the products. Delayed input signals  $x[n - i]$  and coefficients  $a_i$  are the operands of the multipliers in MCMA. The operands of the multipliers in the MCM module are the current input signal  $x[n]$  and coefficients as shown in the transposed form in Fig 1(b). The results of individual constant multiplications go through structure adders (SAs) and delay elements. The digital FIR filters hardware implementations can be classified into two categories: multiplierless based and memory based.



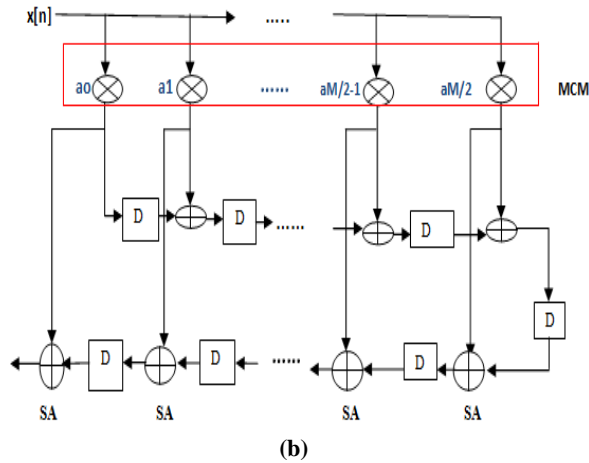


Fig 1 :Structures of linear-phase FIR filters: (a) Direct form and (b) transposed form.

MCM with shift-and-add operations is realized by the multiplierless based designs. The common sub operations is shared using canonical signed digit (CSD) recoding and common sub expression elimination (CSE) minimize the cost of adder in MCM. Two types of approaches [1] are followed in memory based FIR designs: lookup table (LUT) methods and distributed arithmetic (DA) methods. The LUT based design [3] stores odd multiples of the input signal in ROMs in which constant multiplications in MCM is performed. The inner product computation in FIR filter for the bit level partial results is accumulated by the DA based design[4].In this brief, the FIR filter with a new truncated multiplier design is presented which achieves a precised and rounded results. As this method considers the PP reduction, truncation, and rounding the final truncated product satisfies the precision requirement during the design of FIR filter with parallel truncated multiplier.

### Tree Reduction of Parallel Multipliers

PP generation, PP reduction, and final carry propagate addition are the three main steps in design of parallel tree multiplier. PP bits from the multiplicand and the multiplier are produced by PP generation. PP reduction compresses the number of PPs to two, which is summed up by the final addition. Wallace tree and Dadda tree reductions are the two widely used reduction methods. Wallace tree reduction compresses the PPs [5] as early as possible, whereas the Dadda reduction performs compression whenever necessary without increasing the number of carry save addition (CSA) levels. A New reduced area (RA) reduction method [5] has proposed so that the bit width of the final carry-propagate adder (CPA) is minimized.

Table 1 Specifications Of The Two Multiplier Schemes

Multiplier Scheme	FAs	HAs
Dadda tree	38 FAs	8 HAs
Wallace tree	35 FAs	7 HAs

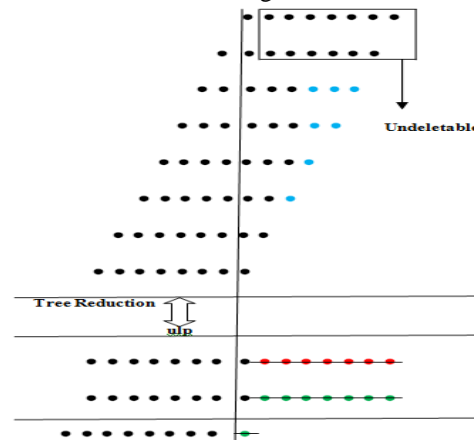
From the above table it is patent that Wallace multiplier contains reduced number of FA and HA. Hence the truncation operation can be made in the Wallace multiplier to design the FIR filter using the truncated Wallace multiplier.

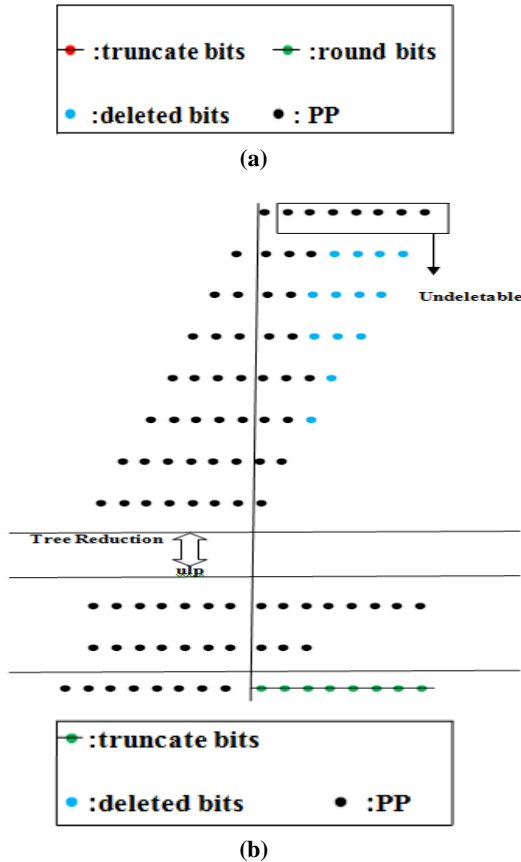
### Proposed Filter Design with Truncated Multiplier

The FIR filter design in the direct form as in Fig. 1 (a) where the MCMA module sums up all the products as  $a_i \times x[n-i]$ . The efficient method of collecting all the PPs into a single PPB matrix with carry save addition is performed where the height of the matrix is reduced to two. Finally the addition is performed by a carry propagate adder in this multiplier.

#### Truncated Multiplier With PP Truncation And Compression

The proposed truncated multiplier consists of several operations such as deletion, reduction, truncation, rounding, and final addition [1]. The first step of deletion operation is performed which removes all the unnecessary PP bits. Those bits are those which are need not to be generated, as shown by the blue dots in Fig 2. An example of  $8 \times 8$  unsigned fractional multiplication is considered here which is in the form of eight product bit truncation. The next step is deletion, where as many possible PP bits are deleted till the deletion error of  $E_D'$  is bounded by  $-1/2 \text{ ulp} \leq E_D' \leq 0$ . The correction bias constant injection [8] of a of  $1/4 \text{ ulp}$  leads the deletion error as  $-1/4 \text{ ulp} \leq E_D' \leq 1/4 \text{ ulp}$ . Per-column reduction is performed after the deletion of PP bits, and two rows of PP bits is generated.





**Fig 2 : 8 × 8 truncated multiplication with eight product bits truncated. (a) Deletion, reduction, and truncation of PP bits. (b) Deletion, reduction, truncation, and rounding plus final addition.**

Next the truncation is performed in which the first row of  $n - 1$  bits from column 1 to column  $n - 1$  is removed, as shown by the crossed red dots in Fig. 2 (a). Truncation error of  $-1/2 \text{ ulp} < E_T \leq 0$  is introduced by truncation. The truncation error is, adjusted by injection of another bias constant [6] of  $1/4 \text{ ulp}$  where the error is bounded by  $-1/4 \text{ ulp} < E_T' \leq 1/4 \text{ ulp}$ . The completion of deletion, reduction, and truncation, the addition of PP bits is done using a CPA which generates the final product of P bits, as shown in Fig 2(b). The bits left after deletion and truncation can be safely removed before final addition as they do not affect the carry bit to column  $n + 1$  during the rounding process. A final bias constant [8] of  $1/2 \text{ ulp}$  is added before addition by CPA to achieve the rounding error as  $-1/2 \text{ ulp} < E_R' \leq 1/2 \text{ ulp}$ . The rounding process involves the removal of bit at column  $n$  after the final CPA. Thus the faithfully rounded truncated multiplier has the total error of  $-\text{ulp} < E = (E_D + E_T + E_R) \leq \text{ulp}$ . As the total error is no more than 1 ulp [6] the proposed truncated multiplier design achieves faithful rounding. Furthermore, the three bias constants  $1_D, 1_T$ , and  $1_R$ , finally can be collected and added as a single

constant bit column  $n + 1$ , as the overall height of the PP matrix should not be increased.

**Delay Element**

The design of FIR filter with direct structure as shown in Fig 1 (a) requires the multiplied output to be delayed using the D flip flop which is widely used in many applications. The D flip flop captures the multiplied output from truncated multiplier at a particular portion of clock cycle. The truth table is as follows. At the rising edge of clock the captured value is given to the final CPA. At falling edge of clock the output of truncated multiplier does not delayed i.e. which does not change.

**Table 2 Truth Table Of D Flip Flop**

Clock	D	Q <sub>next</sub>
Rising edge	0	0
Rising edge	1	1
Non-Rising edge	X	Q

The FIR filter designs based on the transposed structure needs lesser number of adders as it leads to 20% reduction of the total area. But the area of DFFs in the transposed forms is larger. As an example [1] consider the 121-tap filter with 19-bit coefficients and 12-bit signals. The direct form requires only  $12 \times 120 = 1440$  flip-flops, while the transposed form requires 3701 flip-flops. Thus the direct form of FIR filter is designed here which requires lesser number of flip flops.

**Carry Look Ahead Adder**

The completion of FIR filter design requires the addition of two consecutive direct and delayed output by using the Carry look ahead adder. This carry-look ahead adder improves speed of the FIR filter by reducing the amount of time in determining the carry bits. The look ahead adder consists of generate and propagate terms given as follows. Consider here the inputs as A and B

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

The output sum and carry can be defined as

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

$G_i$  is known as the carry generate signal where a carry  $C_{i+1}$  is generated when carry generate signal is one.  $P_i$  is known as the carry propagate signal. Whenever carry propagate signal is 1 the input carry  $C_i$  is propagated to the output carry which shows as  $C_{i+1} = C_i$ . The carries  $C_i$  and  $C_{i+1}$  are created after the generation of carry generate and carry propagate signal.

### Implementation Results

The FIR filter is designed using ISIM simulator with VHDL code and it is also implemented using Xilinx ISE Design Suite 13.2 in FPGA. The simulated screen shot is given in Fig 3.



Fig 3: Screen Shot of Simulated Filter Output

The given input signal x is multiplied with constants a0,a1,a2 and a3 which is delayed and the final addition provides the required output y. After the above mentioned simulation by ISIM it is synthesized.

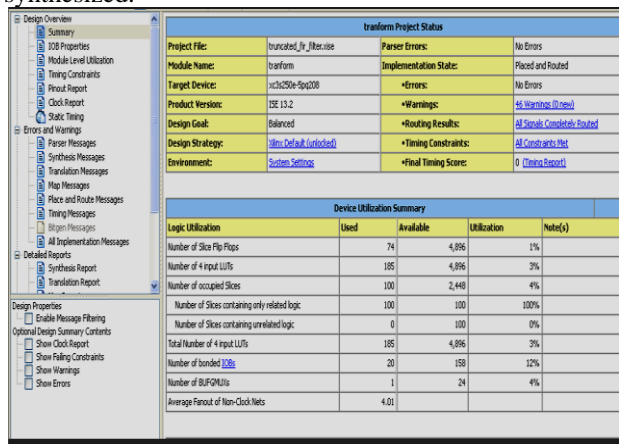


Fig 4 :Area Analysis Of FIR filter

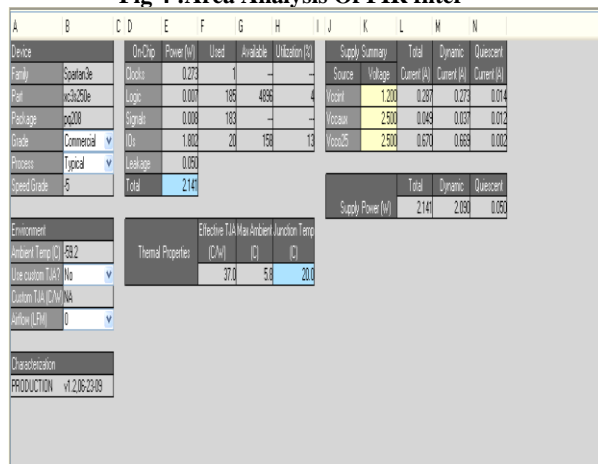


Fig 5 : Power Requirement Of FIR filter

The area, power and delay analysis is shown in the fig 4,5,6 below.

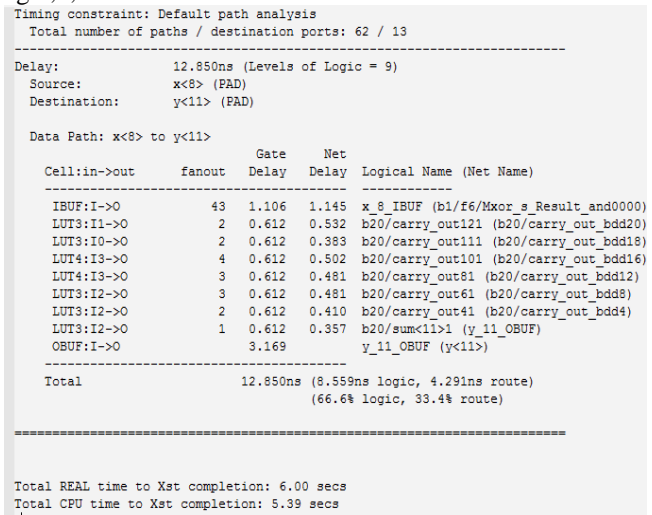


Fig 6 Delay Analysis

The designed FIR filter uses 74 flip flops which is only 1% among the available flipflops with power consumption of about 2.141W and delay is 12.850ns.

### Conclusion and Future Work

This paper describes the design and implementation of low cost FIR filter design using truncated multiplier. The following table provides the comparison between different filter structures using wallace and truncated wallace multiplier. As the number of full adders does not contribute to any area reduction FIR filter design using truncated multiplier which contains lesser number of full adders offers smallest area cost and power consumption. This filter design can be extended by using the Montgomery multiplier.

Table 3 Comparative Result

FIR Filter design method	Number of FA	Number of HA	Structure
Using Wallace Multiplier	69	6	Direct
Using Truncated Multiplier	61	1	Direct

The proposed design [8] involves significantly less area-delay and power-delay complexities compared with the best of the existing designs.

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